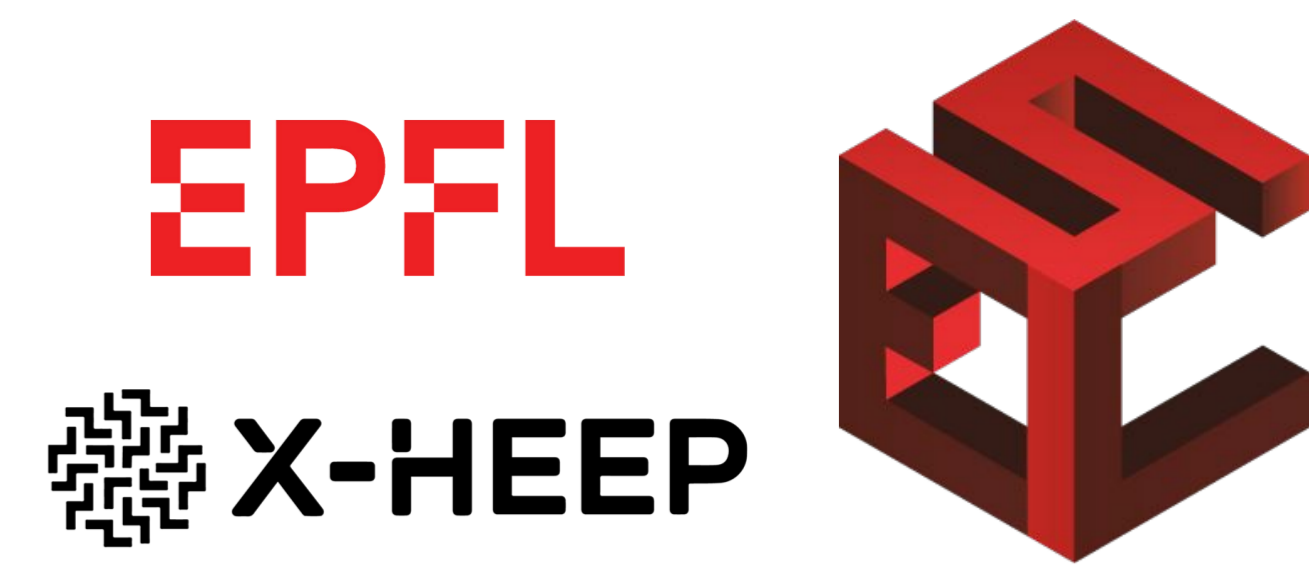# FEMU: An Open-Source RISC-V Emulation Platform for the Exploration of Accelerator-based Edge Applications

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Architecture and Features...

1. Implemented on the Xilinx Zynq-7020 chip on the Pynq-Z2 board

2. Configurable RISC-V CPU:
- CV32E20
- CV32E40P
- CV32E40X

3. Configurable number and size of memory banks

4. Configurable peripherals

5a. Configurable bus topology:
- One-at-a-time
- Fully-connected

5b. Configurable bus addressing:
- Contiguous
- Interleaved
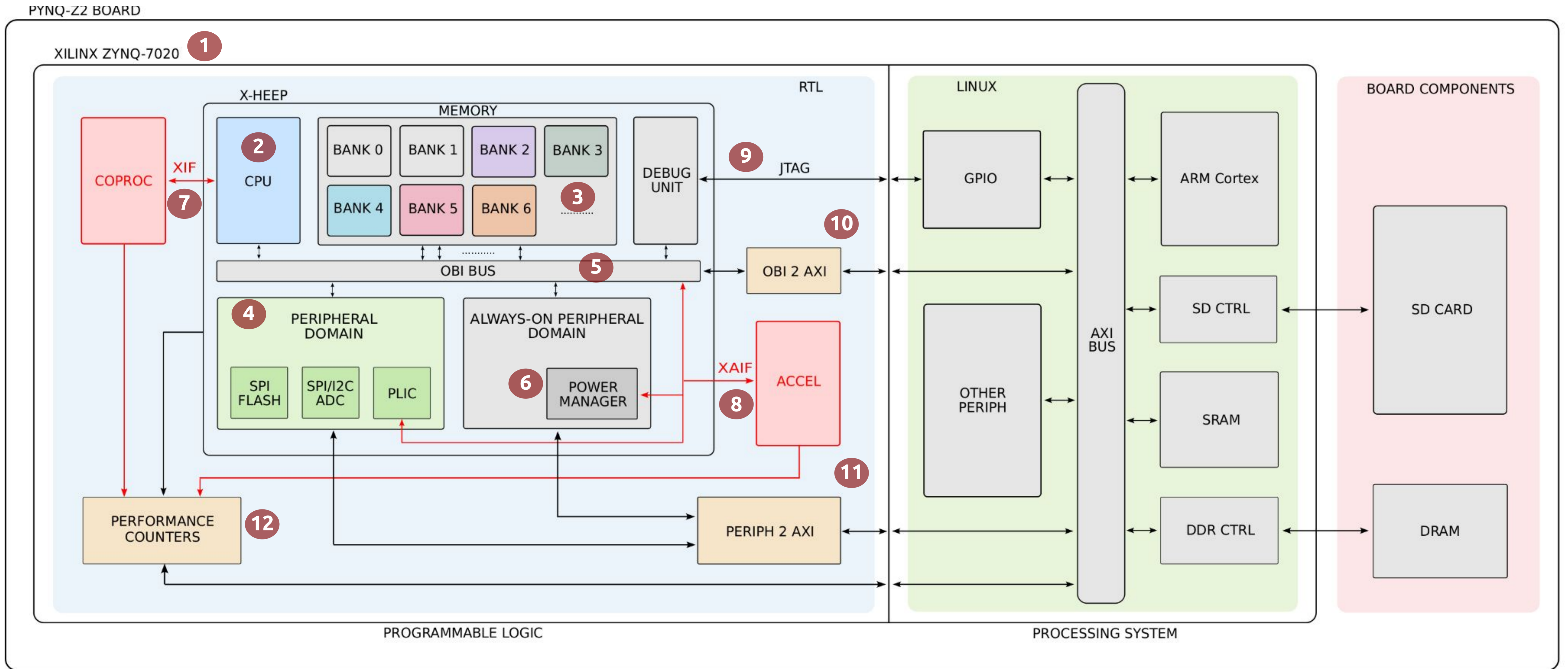
6. Configurable power modes:
- Clock-gating
- Power-gating
- RAM retention

7. XIF: configurable interface to plug coprocessors

8. XAIF: configurable interface to plug accelerators

9. JTAG virtualization on Linux

10. RAM virtualization on Linux: used to expand the X-HEEP RAM size using the board DRAM

11. Peripherals virtualization on Linux: used to perform virtual ADC acquisitions (using SPI, I2C, etc.) from the DRAM or SD card memories

12. Profiling counters: to measure performance and estimate energy

Open-source...

X-HEEP

https://github.com/esl-epfl/x-heep

FEMU-HW

https://github.com/esl-epfl/x-heep-femu

FEMU-SW

https://github.com/esl-epfl/x-heep-femu-sdk

Performance and Energy Estimation...

Performance estimation:

profiling counters measure the time spent by each component of the architecture in each power state during application execution

Energy estimation:

profiling counters values are combined with post-silicon power values from our HEEPocrates chip to estimate the energy consumption of the executed application

HEEPocrates...

Architecture: X-HEEP + coarse-grained reconfigurable array (CGRA) accelerator + in-memory computing (IMC) accelerator

Technology: TSMC 65nm CMOS technology

Application evaluation and optimization:

based on the performance and energy estimation

HEEPocrates